1. Circuitry for processing a communication packet, the circuitry comprising:

a look-up engine configured to transfer a first selector to a content-addressable memory and receive a corresponding first result from the content-addressable memory, generate a second selector based on the first result, transfer the second selector to the content-addressable memory and receive a corresponding second result from the content-addressable memory, retrieve a first context structure based on the second result, build a summation block using the first context structure, and transfer the summation block; and

a processor configured to receive and process the summation block to control handling of the communication packet.

2. The circuitry of claim 1 wherein the processor is configured to process header information from the communication packet to generate and transfer the first selector to the look-up engine.

3. The circuitry of claim 1 further comprising the content-addressable memory configured to receive and process the first selector for a first match and transfer the first result corresponding to the first match and receive and process the second selector for a second match and transfer the second result corresponding to the second match.

4. The circuitry of claim 1 wherein the first context structure relates to one of: network address translation, billing, packet forwarding, packet security, and packet classification

5. The circuitry of claim 1 wherein the look-up engine is configured to generate and transfer a third selector to the content-addressable memory based on the first result and receive a corresponding third result from the content-addressable memory, retrieve a second context structure based on the third result, and build the summation block using the second context structure.

6. The circuitry of claim 1 wherein the first result indicates a selector modification and the look-up engine is configured to generate the second selector based on the selector modification.

7. The circuitry of claim 1 wherein the first result indicates a series of selector modifications and the look-up engine is configured to generate the second selector and additional selectors based on the series.

8. The circuitry of claim 1 wherein the first result indicates an instruction and the look-up engine is configured to implement the instruction.

9. The circuitry of claim 8 wherein the instruction is to store the summation block for subsequent use.

10. The circuitry of claim 1 wherein the processor, the look-up engine, and the content-addressable memory are configured on a single integrated circuit.

11. A method of operating circuitry to process a communication packet, the method comprising:

transferring a first selector to a content-addressable memory;

receiving a corresponding first result from the content-addressable memory;

generating a second selector based on the first result;

transferring the second selector to the content-addressable memory;

receiving a corresponding second result from the content-addressable memory;

retrieving a first context structure based on the second result;

building a summation block using the first context structure; and

processing the summation block to control handling of the communication packet.

12. The method of claim 11 further comprising processing header information from the communication packet to generate the first selector.

13. The method of claim 11 further comprising in the content-addressable memory:

receiving and processing the first selector for a first match;

transferring the first result corresponding to the first match;

receiving and processing the second selector for a second match; and

transferring the second result corresponding to the second match.

14. The method of claim 11 wherein the first context structure relates to one of: network address translation, billing, packet forwarding, packet security, and packet classification

15. The method of claim 11 further comprising:

generating and transferring a third selector to the content-addressable memory based on the first result;

receiving a corresponding third result from the content-addressable memory;

retrieving a second context structure based on the third result; and

building the summation block using the second context structure.

16. The method of claim 11 wherein the first result indicates a selector modification and wherein generating the second selector comprises generating the second selector based on the selector modification.

17. The method of claim 11 wherein the first result indicates a series of selector modifications and wherein generating the second selector comprises generating the second selector and additional selectors based on the series.

18. The method of claim 11 wherein the first result indicates an instruction further comprising implementing the instruction.

19. The method of claim 18 wherein the instruction is to store the summation block for subsequent use.

20. The method of claim 11 wherein the circuitry and the content-addressable memory are configured on a single integrated circuit.